**National University of Computer and Emerging Sciences**

**(Islamabad Campus)**

Department of Computer Science

**Signature of Invigilator: \_\_\_\_\_\_\_\_\_\_\_\_\_\_ Serial No:\_\_\_\_\_\_\_\_\_**

EE-105 Computer Logic Design

Final Examination (Spring 2013)

**Instructor(s):**

Dr Ayub Alvi, Ms Mehreen Alam, Mr Adnan Saeed

Monday May 27, 2013

**Total Marks: 105 Time Allowed: 3 hour**

Please read the instructions carefully:

1. Understanding the question paper is also part of the exam, so do not ask any clarification.
2. Solve questions in the space provided, or if you need more space write on the back side of the paper and clearly mark question and part number etc.
3. It is a CLOSED book/notes exam.
4. Calculators are NOT allowed.
5. Write your name and roll number on each page.
6. The question paper is printed on both sides of the pages.
7. Use permanent ink pens only. Any part done using soft pencil will not be marked and cannot be claimed for rechecking.

**Roll No: \_\_\_\_\_\_\_\_\_ Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Signature\_\_\_\_\_\_\_\_\_\_\_\_ Sec: \_\_\_**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Question | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | Total |
| Total Marks | 15 | 9 | 15 | 15 | 15 | 10 | 13 | 13 | 105 |
| Marks Obtained |  |  |  |  |  |  |  |  |  |

Vetted By: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Vetter Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Question # 1[15 = 5,5,5]**

1. Complete the following table :

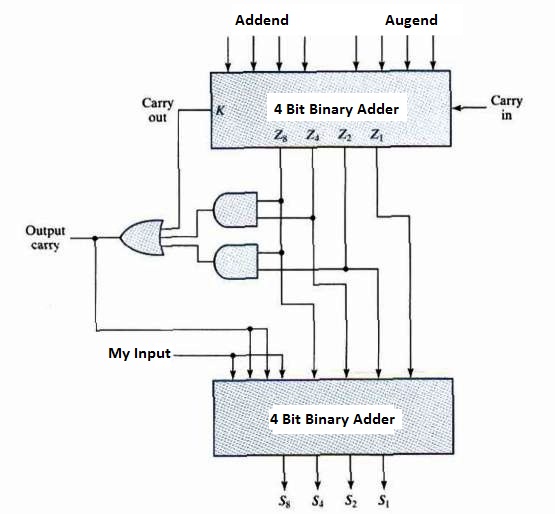
|  |  |  |  |
| --- | --- | --- | --- |
| Binary | Octal | Decimal | Hexadecimal |
| 1011.0011 |  |  |  |
|  |  | 29.99 |  |
|  |  |  | 1B |

1. Calculate the following:
2. 11001 plus 101
3. 11010 minus 10101 using 2’s complement representation
4. 1101 times 1001
5. 101101 divided by 110
6. Complete the following table, Use binary numbers with a sign bit plus 5 bits for the magnitude.

|  |  |  |  |
| --- | --- | --- | --- |
| Decimal | Sign Magnitude | Two’s Complement | One’s Complement |
| -11 |  |  |  |
| 6 |  |  |  |
| -1 |  |  |  |

**Question # 2[9 = 3, 6]**

1. Construct a 5-32 line decoder with two 4-16 line decoders with enable. Use block diagram for components.
2. For the following circuit, complete the table below assuming ‘Carry In’ is zero.



|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **My Input** | **Addend** | **Augends** | **Z8Z4Z2Z1** | **S8S4S2S1** | **Output Carry** |
| 0 | 0111 | 0111 |  |  |  |
| 1 | 1110 | 0110 |  |  |  |

**Question # 3 [15 = 6,9]**

1. Write the characteristic equations and draw the excitation tables for D, T and JK flip-flops.
2. A sequential circuit has two JK flip flops A and B, two inputs x and y. The FF input equations and circuit output equations are:
3. Draw the logic diagram of the circuit.
4. Tabulate the state table.
5. Draw the state diagram

**Question # 4 [15 = 10,5]**



1. A sequential circuit has three flip-flops, one input and one output. Its state diagram is shown in figure on the right.
2. Derive State Table from the State Diagram. Treat the unused states as don’t cares.
3. Derive Sate Equations from the State Table using D flip flops.
4. Draw the resultant circuit.
5. Does the circuit malfunction for taking the unused states as don’t cares? Justify.
6. Can the number of states in the table below be reduced? If yes, draw the reduced state table, else state reasons.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Next State** | | **Output** | |
| **Present State** | **X=0** | **X=1** | **X=0** | **X=1** |
| *a* | *f* | *b* | *0* | *0* |
| *b* | *d* | *c* | *0* | *0* |
| *c* | *f* | *e* | *0* | *0* |
| *d* | *g* | *a* | *1* | *0* |
| *e* | *d* | *c* | *0* | *0* |
| *f* | *f* | *b* | *1* | *1* |
| *g* | *g* | *h* | *0* | *1* |
| *h* | *g* | *a* | *1* | *0* |

**Question # 5 [15 = 8, 3, 4]**

1. Design a synchronous counter with T-flip flops that goes though the following binary repeated sequence: 0,2,3,4,5,6. Consider the unused states as don’t cares. Show that when binary states 001 and 111 are taken as don’t care conditions, the counter may not operate properly.
2. Draw (do not design) and label the logic diagram for a 3-bit ripple counter implemented with T flip flops.
3. Design a 3-bit synchronous counter (0, 1,2,3,4,5,6,7...) with J-K flip flops.

**Question # 6 [10 = 5,5 ]**

1. Given four D flip-flops and four 4 x 1 multiplexers construct a 4-bit universal shift register that operates according to the following function table using mode selection inputs S1 and S0. (Draw appropriate lines enabling the register to work according to the table given below)

|  |  |  |
| --- | --- | --- |
| S1 | S0 | Register Operation |
| 0 | 0 | Parallel load |
| 0 | 1 | Shift left |
| 1 | 0 | No change |
| 1 | 1 | Shift right |

4 x 1

Mux

3 2 1 0

D FlipFlop

D

D FlipFlop

D

D FlipFlop

D

D

D FlipFlop

D

D

4 x 1

Mux

3 2 1 0

4 x 1

Mux

3 2 1 0

4 x 1

Mux

3 2 1 0

A0

A1

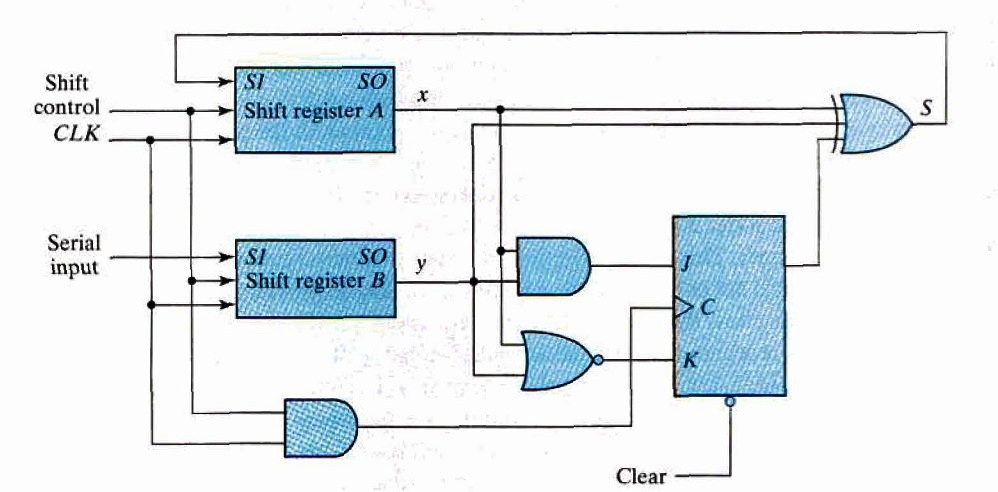
A2

A3

S1

S0

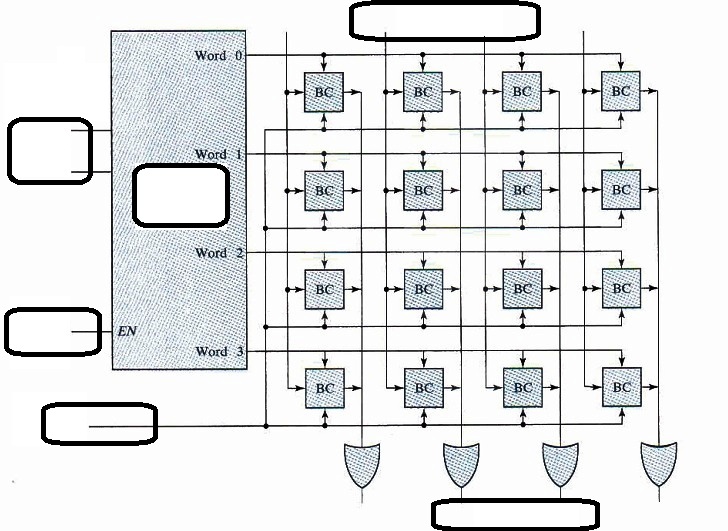
1. In the diagram below, assume that the 4-bit shift register A contains 1001 and Shift register B is empty (0000), What will be the contents of register A and Register B after three clock cycles given that Serial Input for Register B is connected to a logic high.



**Question # 7 [13 = 2,2,3,2,4]**

Random Access Memory (RAM) is a collection of storage cells in which time taken to access information from any location remains the same.

1. How may 32K x 8 RAM chips are needed to provide a total memory capacity of 256K x 8?
2. How many address lines are required to access 256K bytes?
3. How many of these lines are directly connected to the address lines of all the chips?
4. How many address lines must be decoded for the chip select inputs? Specify the size of the decoder.
5. Label the following diagram of a 4x4 RAM



**Question # 8 [13 = 4,4,5]**

Hamming Error Detection and correction scheme is used for four data bits: D3, D5, D6, D7 together with three parity bits: P1, P2 and P4. Assume the data word 0010.

1. Evaluate the 7-bit composite code word.
2. Evaluate three check bits C4, C2 and C1 assuming no error.
3. Assume an error in bit D5 during writing into memory. Show how the error in the bit is detected and corrected.